

WHAT IS CLAIMED IS:

- Summary
1. ~~A method of coupling a plurality of signals to a plurality of destinations, comprising the steps of:~~
 - assigning a priority to each signal of the plurality of signals;
 - 5 coupling the signals to a routing circuit so that ones of the signals can be routed to different destinations; and
 - coupling said signals through said routing circuits so that said signals are routed to respective destinations as a function of the priority assigned to said signals.
 2. The method of Claim 1, further including assigning a priority to each said destination so that a highest priority signal is coupled by said routing circuit to a highest priority destination.
 3. The method of Claim 1, further including enabling said routing circuit to control whether signals are to be routed therethrough.
 4. The method of Claim 3, further including shifting lower priority signals to different destinations when a signal is not routed through said routing circuit.
 5. The method of Claim 4, further including shifting signals to destinations to make the used destinations contiguous.
 6. The method of Claim 1, further including routing signals through said routing circuit in a bi-directional manner.

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7. ~~The method of Claim 1, further including establishing a priority route through said routing circuit for routing a plurality of different signals therethrough.~~

8. The method of Claim 7, further including using digital logic to carry out said routing in said routing circuit.

9. The method of Claim 1, further including routing a signal through a plurality of routing cells arranged in at least one row and in at least one column, from an input of said routing circuit to an output of said routing circuit.

10. The method of Claim 9, further including routing a signal through a first routing cell to an output if said first routing cell is enabled, and routing the signal to a second routing cell if the first routing cell is disabled.

11. The method of Claim 10, further including enabling the first routing cell of the routing circuit to transfer a signal coupled thereto to an output of the routing circuit, and further including generating a control signal to disable a neighbor routing circuit.

12. The method of Claim 1, further including using a digital controller to route signals from a plurality of digital resources through the routing circuit to a plurality of pins.

13. The method of Claim 12, further including routing signals in a bidirectional manner through said routing cell.

14. A method of coupling a plurality of signals to a plurality of destinations based on priority, comprising the steps of:

assigning a priority to a plurality of inputs of a routing circuit;

assigning a priority to a plurality of outputs of a routing circuit;

coupling signals to one or more respective inputs of said routing circuit;

enabling ones of said signals to be coupled through said routing circuit and disabling other signals and preventing said other signals from being routed to an output of said routing circuits; and

routing said enabled signals through said routing circuit to a respective output as a function of priority.

15. ~~The method of Claim 14, further including routing signals through a plurality of routing cells from an input of said routing circuit to an output of said routing circuit.~~

16. ~~The method of Claim 15, further including routing signals through routing cells arranged in rows and columns, and further including applying said signals to respective input routing cells in different rows, and extracting signals from output routing cells arranged in different columns.~~

17. ~~A routing circuit for routing a plurality of signals to a corresponding~~
plurality of destinations, comprising:

a matrix of routing cells, said matrix having a plurality of signal inputs and a plurality of signal outputs; and

5 said signal inputs to said matrix being assigned a priority such that signals coupled to high priority inputs can be routed through one or more of said routing cells to a given number of signal outputs, and lower priority signals can be routed through one or more routing cells to a greater number of signal outputs.

18. The routing circuit of Claim 17, further including circuits in said routing cells for changing the routing of signals to different signal outputs.

19. The routing circuit of Claim 18, further including a select circuit for selecting ones of said routing cells, said select circuit being effective to select an input signal for routing through said matrix.

20. The routing circuit of Claim 19, wherein said select circuit is responsive to one logic state to route selected signals through said matrix, and responsive to a second logic state for inhibiting non-selected signals from being routed through said matrix.

21. The routing circuit of Claim 20, wherein said matrix includes routing cells responsive to said second state for shifting other selected input signals from one output to another output.

22. The routing circuit of Claim 17, wherein ones of said routing cells of a column have respective outputs coupled to a logic circuit for providing a common column output, said common column output coupled to a pin driver.

23. ~~The routing circuit of Claim 22, wherein each said routing cell of a column has a circuit for enabling a cell output thereof.~~

24. The routing circuit of Claim 23, wherein ones of said routing cells in a column have a disabling circuit for disabling other routing cells in the respective column.

25. The routing circuit of Claim 17, wherein each said routing cell of a row receives the same signal input.

26. The routing circuit of Claim 25, wherein each routing cell of a row receives a common select signal for selecting whether the input signal to the row is to be coupled to an output of the matrix.

27. The routing circuit of Claim 17, wherein ones of said routing cells have logic circuits for carrying signals in a bidirectional manner between signal resources and I/O pins.

28. The routing circuit of Claim 17, wherein ones of said routing cells each have a priority encoding circuit that routes a high priority signal to a predetermined output, and disables lower priority signals from reaching said predetermined output.

29. The routing circuit of Claim 28, wherein the disabled routing cells couple lower priority signals to other routing cells for routing to other outputs.

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30. ~~The routing circuit of Claim 29, wherein said priority encoding circuit~~
is coupled to other routing cells in a column of the matrix for disabling thereof, and
said priority encoding circuit is effective to couple lower priority signals to other
routing cells of a row in the matrix.

31. The routing circuit of Claim 17, further including a circuit in ones of
said routing cells for carrying a signal to determine whether an I/O pin is to be
utilized as an output or an input.

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32. A routing circuit for routing a plurality of signals to a corresponding plurality of destinations, comprising:

5 a matrix having rows and columns of routing cells;
each said row of routing cells associated with a different signal input;
each said column of routing cells associated with a different output;
said routing cells having circuits for automatically routing N signals ranked in priority to N consecutive outputs, and if N-1 signals of the N signals are routed through said matrix of routing cells, then the N-1 signals are routed to N-1 consecutive outputs.

33. The routing circuit of Claim 32, wherein said routing cells are configured to route the signals to consecutive outputs, starting with a highest priority output.

34. The routing circuit of Claim 32, further including coupling N signals to said signal inputs of the matrix, and selecting for operation less than N signals to be routed through said matrix.

35. The routing circuit of Claim 32, further including providing bidirectional signal paths through said routing cells.

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36. ~~A routing circuit for routing a plurality of signals to a corresponding plurality of destinations, comprising:~~

~~a matrix having rows and columns of routing cells;~~
~~each said row of routing cells associated with a different signal input;~~
~~each said column of routing cells associated with a different output;~~
~~at least one routing cell of said matrix including a logic circuit in a column for receiving a select signal to enable coupling an input signal to an output of the matrix, and said logic circuit disabling other routing cells in the column from coupling respective input signals to that output.~~

37. ~~The routing circuit of Claim 36, wherein said one routing cell includes a circuit responsive to a disable signal for enabling other routing cells in a row associated with said one routing cell.~~

38. ~~The routing circuit of Claim 36, further including a multi-input logic circuit for receiving an output of each routing cell of a column.~~

39. ~~The routing circuit of Claim 36, wherein said matrix includes a lack of a routing cell at one or more intersections of the rows and columns of said matrix.~~

40. ~~The routing circuit of Claim 36, further including a circuit for receiving outputs of said matrix, and for receiving data signals not coupled through said matrix.~~

41. ~~The routing circuit of Claim 36, further including in combination a microprocessor and plural chip terminal pins integrated with said routing circuit on a semiconductor chip.~~

42. The routing circuit of Claim 41, further including a plurality of signal resources coupled to respective signal inputs of said matrix, and said terminal pins receive output signals from said matrix.

43. The routing circuit of Claim 42, further including a register controlled by said microprocessor for selecting which signal resources are to be routed through said matrix.

44. The routing circuit of Claim 36, further including a circuit responsive to a cell disabling signal from said matrix for carrying signals from a microprocessor to an I/O pin without passing through said matrix.

45. The routing circuit of Claim 36, further including a pin driver circuit associated with each output of said matrix, and including a circuit responsive to a signal for controlling each said pin driver circuit so that an output of each pin driver circuit can be driven to a high impedance state.

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